REMARKS

In response to the Office Action, Applicant respectfully requests the Examiner to reconsider the above-captioned application in view of the foregoing amendments and the following comments.

Discussion of Claim Rejections Under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected Claims 1, 2, 4-12, 14-16, 18-26, 28-39, and 40-49 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,914,727, to Horan (hereinafter "Horan"), et al. and U.S. Patent No. 5,869,101, to Arimilli, et al. (hereinafter "Arimilli"). Claims 3 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Horan and Arimilli in view of U.S. Patent No. 6,002,411, to Dye. Claims 13 and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Horan and Arimilli in view of U.S. Patent No. 6,118,462, to Margulis (hereinafter "Margulis"). Claim 50 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Horan, Arimilli, and Dye.

Claims 1, 14, 28, and 48

Applicant respectfully disagrees with these rejections. Claim 1 recites "at least two memory controllers for controlling a main memory, wherein a first of the at least two memory controllers is directly connected to a central processing unit bus, a bus supporting a peripheral device, and the main memory, and also wherein the first of the at least two memory controllers comprises an accelerated graphics port for establishing a dedicated point-to-point connection between the first of the at least two memory controllers and an accelerated graphics processor." Independent Claims 14, 28, and 40 each include similar types of limitations.

To establish a *prima facie* case of obviousness a three-prong test must be met. First, there must be some suggestion or motivation, either in the references or in the knowledge generally available among those of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success found in the prior art. Third, the prior art reference must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991). Applicant respectfully submits that there is no motivation to combine the references as suggested by the Examiner and that the cited references, even if combined, fail to describe or suggest all of the claimed limitations.

Horan is generally directed to a system for providing a logic chipset that functions between a bridge and a memory controller. In Horan, a central processing unit 102 is connected to a core logic chipset 204 through a memory bus 204. *See* Horan, col. 10, lines 47-49. As was recognized by the Examiner in the Office Action, Horan describes a single controller for controlling the main memory, i.e., memory interface and control 304.

Arimilli describes a symmetric multiprocessor system comprising multiple partial system memories 18a-18n and corresponding memory controllers 17a-17n. In Arimilli, each of the CPUs includes a memory controller 17b. *See* Figure 2 and col. 2, lines 6-8. In the Office Action, the Examiner stated that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Horan and Arimilli whereby the symmetric multiprocessor system contemplated by Horan is implemented with multiple memory controllers and associated system memory as taught by Arimilli in order to provide the benefits of scalability and parallel bus traffic between the memory controller and the system memory. Applicant respectfully submits that there is no motivation to combine the references as suggested by the Examiner. Furthermore, Applicant respectfully submits that even if they were combined, such combination would not anticipate or make obvious the claimed invention.

Applicant notes that there is no suggestion of a need in Horan to improve the scalability and parallel bus traffic between the core logic 204 and the system RAM 106. Although Horan indicates that multiple CPUs may be used in a computer, it is primarily directed to disabling allocation of accelerated graphics port (AGP) memory space when no AGP device is present. *See Horan*, Title and col. 6, lines 9-20. In contrast, Arimilli is directed to providing a scalable multi-processor architecture. Applicant submits that Arimilli does not describe the usage of AGP devices and memory controllers for supporting same. Applicant submits that the prior art must suggest the desirability of the claimed invention. *See* M.P.E.P. § 2143.01. The fact that references can be modified is not sufficient to establish prima facie obviousness. *Id.* Furthermore, the fact that the claimed invention is within the capability of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness. *Id.* In this case, the Examiner has merely made conclusory findings regarding the motivation to modify the cited references. In Horan, there is no suggestion of a need to improve processor scalability or improve bus traffic between the core logic 204 and the RAM 106. Furthermore, Applicant respectfully submits that contrary to the of the design tenets of AGP with respect to increasing

speed, moving the memory controller into the processor, could cause the processor to be a bottleneck for memory transactions when it is processing non-graphic related data.

Furthermore, even if Horan was combined with Arimilli, Applicant respectfully submits that such combination would not describe or suggest all of the cited claim limitations. If the memory controller 17 of Arimilli was incorporated into the central processing unit 102 of Horan, the memory controller would be connected to a single bus, i.e., the host bus. The memory controller would not be directly connected to the central processing unit bus *and* a bus supporting a peripheral device, as is claimed.

For the foregoing reasons, Applicant respectfully submits that Applicant respectfully submits that there is no motivation to combine the reference as suggested by the Examiner and that the cited references, even if combined, fail to describe or suggest all of the claimed limitations.

Claims 2-13, 15-27, 29-39, and 41-50

Since Claims 2-13, 15-27, 29-39, and 41-50, each depend on one of Claims 1, 14, 28, and 40, Applicant respectfully submits that these claims are allowable for at least the reasons discussed above and the subject matter of their own limitations.

Summary

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above amendments and remarks, reconsideration and withdrawal of the outstanding rejections is respectfully requested. If the Examiner has any questions which may be answered by telephone, he is invited to call the undersigned directly.

Respectfully submitted,

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